

PTO/SB/08A
Substitute for Form PTO-1449

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 5

Application Number 72804

Filing Date January 11, 2002

First Named Inventor Chason et al.

Art Unit 2811

Examiner Name Jones, J.

Attorney Docket 72804

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ²			
JMD		US-6,395,124	5/28/02	Oxman et al.	
JMD		US-6,276,278	4/23/02	Egawa et al.	
JMD		US-6,352,881	3/5/02	Nguyen et al.	
JMD		US-6,352,878	3/5/02	Mostafazadeh et al.	
JMD		US-6,335,571	1/01/02	Capote et al.	
JMD		US-6,341,418	1/29/02	Brouillette et al.	
JMD		US-6,323,062	11/27/01	Gilleo et al.	
JMD		US-6,297,560	10/2/01	Capote et al.	
JMD		US-6,287,893	9/11/01	Elenius et al.	
JMD		US-6,245,595	6/12/01	Nguyen et al.	
JMD		US-6,238,223	5/29/01	Cobbley et al.	
JMD		US-6,194,788	2/27/01	Gilleo et al.	
JMD		US-6,171,887	1/9/01	Yamaji	
JMD		US-6,168,972	1/02/01	Wang et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵				
JMD		WO 99/03597	1/28/99			
JMD		WO 99/04430	1/28/00			
JMD		WO 99/56312	11/4/99			
JMD		WO 00/54322	9/14/00			
JMD		WO 01/20658 A1	3/22/01			

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	72804		
		Filing Date	January 11, 2002		
		First Named Inventor	Chason et al.		
		Art Unit	2811		
		Examiner Name	Jones, J.		
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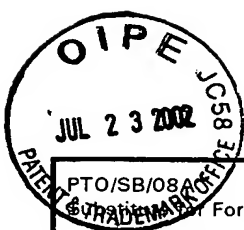
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		Number-Kind Code ²			
JMN		US-6,132,656	10/17/00	Zhou et al.	
JMN		US-6,121,689	9/19/00	capote et al.	
JMN		US-6,075,290	6/13/00	Schaefer et al.	
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JMN		US-5,985,456	11/16/99	Zhou et al.	
JMN		US-5,985,043	11/16/99	Zhou et al.	
JMN		US-5,956,605	9/21/99	Akram et al.	
JMN		US-5,925,936	7/20/99	Yamaji	
JMN		US-5,814,401	9/29/98	Gamota et al.	
JMN		US-5,128,746	7/7/92	Pennisi et al.	
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JMN		US-2002/0014703 A1	2/7/02	Capote et al.	
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PTO/SB/08A US Patent and Trademark Office Form PTO-1449		Application Number	72804		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	January 11, 2002		
		First Named Inventor	Chason et al.		
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		Examiner Name	Jones, J.		
Sheet	3	of	5	Attorney Docket	72804

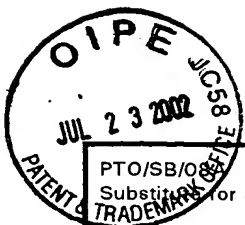
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
JMB		Robert V. Burress et al., "A Practical, Flip-Chip, Multi-layer Pre-Encapsulation Technology for Wafer-Scale Unterfill," IEEE, 5 pages (2001)	
JMB		Y. Joon Lee et al., "Cyanate-Bismaleimide-Epoxy Resin Compositions for Flip Chip, BGA and CSP Pre-Encapsulation," International Conference on High-Density Interconnect and Systems Packaging, pg. 76-81 (2001)	
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JMB		Marc Chason, "Development of Wafer Scale Applied Reworkable Fluxing Underfill for Direct Chip Attach," APEX, 19 pages (2001)	
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JMB		Jing Qi et al., "Assembly of Flip Chips Utilizing Wafer Applied Underfill," APEX, 7 pages (2002)	

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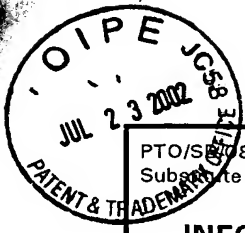
PTO/SB/08 Substitution for Form PTO-1449		Application Number	72804
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS		
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JMD		Dr. Larry Crane et al., "Making Direct Chip Attach Transparent to Surface Mount Technology," Chip Scale Review pg. 50-53 (1999)
JMD		Mr. Albert Capote et al., "A Novel Flip-Scale package Using Pre-Applied Multilayer Flip-Chip Under-Encapsulation," Pan Pacific Microelectronics Symposium pg. 153-158 (1999)
JMD		Dr. Ken Gilleo et al., "Wafer-Level Flip Chip: Bumps, Flux and Underflip," HDI pg. 22-27 (1999)
JMD		Dr. Ken Gilleo et al., "Transforming Flip Chip into CSP with Reworkable Wafer-Level Underfill," Pan Pacific Microelectronics Symposium pg. 159-165 (1999)
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JMD		C. Dustin Johnson, et al., "Wafer Scale packaging Based on Underfill Applied at the Wafer Level for Low-Cost Flip Chip Processing," IEEE, 6 pages (1999)
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JMD		Wayne Johnson, Ph.D. et al., "Wafer Applied Underfills for Flip Chip Assembly," ICAPS, 11 pages (2002)	
JMD		Q. Tong et al., "Novel Materials and Processes for Wafer Pre-Apply Flip Chip and Chip Scale Packaging," IEEE, 6 pages (2002)	
JMD		Q. Tong et al., "Encapsulant Materials and Processes for Wafer Level-Chip Scale Packaging (WL- CSP)," IEEE, 7 pages (2002)	
JMD		Robert V. Burress et al., "A Novel, Wafer-Scale Technology for Addressing Process and Cost Obstacles Associated with Unterfilling FCOB," IEEE, 4 pages (2002)	

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